METHOD AND APPARATUS FOR COMPENSATING DC OFFSETS IN COMMUNICATION SYSTEMS

[0001] This application is a continuation-in-part of copending U.S. patent application serial number 10/600,499, filed June 19, 2003, which claims priority to U.S. provisional patent application serial number 60/390,585, filed on June 20, 2002.

[0002] Figure 1 is a block diagram of a wireless data communications system 10, which includes a transmitter 12 and a receiver 14. At the transmitter 12, as a user 16 speaks into a microphone 18, it converts the sound energy of the user's voice into analog electrical signals having a real-time voltage waveform 20. Although the example shown is described in terms of converted sound energy of a user's voice, the operation of the transmitter 12 is the same, or substantially the same, with respect to other types of signals as well. With appropriate modifications, the transmitter 12, as well as the receiver described below, may also be used to transmit and receive digital signals, the analog embodiment being shown only by way of example.

[0003] With reference again to the analog embodiment, a sampler 22 converts the analog electrical signals into discrete electrical signals to provide a sampled waveform 24. A quantizer 26 quantizes the discrete electrical signals into pulse amplitude modulation voltages, representing a quantized waveform version of the sampled waveform 28. An encoder 30 encodes the quantized discrete electrical signal into a string of bits, for example, represented by a stream of eight bit words, or octets 32. The octets are encoded by a symbol encoder 34 according to a symbol encoding scheme. Thus, for example, the symbol encoder 34 encodes each successive two bits of each octet to provide a stream of two bit symbols.

[0004] The symbols produced by the symbol encoder 34 represent the values of $I_{component}$ and $Q_{component}$ vectors such that their vector sum results in an appropriate value under the defined signal scheme. The $I_{component}$ vector is multiplied in multiplier 38 by a first sine wave produced by oscillator 40 to produce a modulated "in-phase" (I) signal. On the other hand, the $Q_{component}$ vector is multiplied in multiplier 42 by a second sine wave produced by the oscillator 40 that has been shifted 90° by a 90° phase shifter 44 to produce a modulated "quadrature-phase" (Q) signal. The I and Q modulated signals are added by an adder 46 together with the sine wave produced by oscillator 40 to produce a

composite signal, which is received by modulator 48 to modulate a carrier sine wave. The modulator 48 includes an oscillator 50 and multiplier 52, which multiplies the composite and the oscillator signals to produce the modulated carrier signal, which is then transmitted by an antenna 54.

[0005] At the receiver 14, the transmitted signal is received by an antenna 60, which feeds the received signal into a low noise amplifier (LNA) 62, the output of which is connected to a mixer 64. The mixer 64 includes a multiplier 66 and oscillator 68 arranged to produce quadrature output signals on lines 70 and 72. The signals on lines 70 and 72 are connected to a filter and automatic gain control unit (AGC) 74. The filter and AGC unit 74 automatically adjusts the gain applied to the output signals from the AGC 74 as a function of the strength of the modulated carrier received via antenna 60, in order to maintain a relatively constant output signal level.

[0006] The quadrature output signals from the filter and AGC unit 74 are connected through a subtracter 80, below described in detail, to a symbol demodulator 76, which demodulates the automatic gain controlled version of the received signal to produce both the in-phase (I) signal and the quadrature-phase (Q) signals, which respectively represent the received values of the $I_{component}$ vector and $Q_{component}$ vector signals. Thereafter, a symbol decoder 78, which may be a quadrature phase shifted keyed (QPSK) decoder, uses the two bit values of the $I_{component}$ and $Q_{component}$ vectors to produce the decoded successive symbol bits in a stream of reconstructed octet words. The reconstructed octet words are then passed to D/A converter 79, which outputs an analog electrical signal which is converted into sound energy by speaker 81. In processing a digital signal, the output from the signal decoder may be separately processed, without need for the D/A converter 80.

[0007] Referring additionally now to Figure 2a, a map of the I and Q inputs to the symbol decoder 76 in an "ideal," or theoretical, system, are shown. In the ideal system, both the I and Q components are always detected correctly by the symbol decoder 78. For instance, in the example shown, respective I and Q values "0" and "1" are properly decoded as "01".

[0008] However, in an actual, physical system, an example of the signal map of which is shown in Figure 2b, without the use of the subtracter 80 system irregularities give rise to direct current (DC) offset voltages on either or both the I and Q components. Factors that may cause the values of the I and Q value to contain a DC offset, for example,

include the presence of noise and variations of the signal strength of the received signal, as well as component and circuit imbalances and designs in the receiver system. Moreover, due to the effects of the AGC 74, the DC offsets will tend to vary over time. Such time-varying DC offsets may be difficult to compensate.

[0009] Insofar as symbol decoder 78 relies upon both the sign and magnitude of the detected voltages of the respective I and Q components in order to correctly decode a received symbol, the presence of DC offset voltages can result in symbol decoder 78 incorrectly decoding a received symbol. In the example shown, for example, the respective values for I and Q of "0" and "1" shown in Figure 2a have erroneously been detected as "00", shown in Figure 2b.

[0010] The DC offsets which may be present in the received signals, however, can be substantially reduced or eliminated, regardless of whether AGC 74 is causing such DC offsets to change over time, through the use of the subtracter 80 and methods illustrated in the block diagram of Figure 3, to which reference is now additionally made.

[0011] The subtracter 80 is placed between the filter & AGC 74 and the symbol demodulator 76 and symbol decoder 78 in the receiver portion of the system 10 (the symbol demodulator 76 and symbol decoder 78 being represented for convenience as a single block 96). Briefly, in the subtracter 80, a time-averaged value of the DC offsets of both I and Q components are substantially removed or eliminated before symbol decoding is performed.

[0012] In the subtracter 80, the demodulated in-phase $I_{component}$ signal on line 82 is fed into an $I_{component}$ DC estimator 88. The DC estimator 88 determines an instantaneous DC level in the $I_{component}$ signal, such as through low pass filtering techniques, or the like. The output of the $I_{component}$ DC estimator 88 is fed into an $I_{component}$ DC averager 90, which calculates a time-average of its DC input. The average may be calculated and updated periodically, for example, over successive predetermined time intervals, or may be maintained as a running average over a predetermined number of preceding average calculated values, or may be performed by another averaging technique. One way by which the average may be calculated, for example, is by summing a predetermined number of output values from the DC estimator 88 and calculating a mean value.

[0013] The output of the $I_{component}$ DC averager 90 is fed into the DC component subtracter 86, which subtracts the time-averaged DC component from the demodulated in-phase $I_{component}$ signal on line 82. The output of the DC component subtracter 86

$I'_{component}$, which represents the $I_{component}$ value having any DC offset that may be contained therein substantially removed, then is fed into the symbol demodulator and decoder 96.

[0014] At the same time, in the quadrature signal channel, the demodulated quadrature-phase $Q_{component}$ signal on line 98 is fed into a $Q_{component}$ DC estimator 104. The DC estimator 104 determines an instantaneous DC level in the $Q_{component}$ signal, using techniques described above with respect to the $I_{component}$ DC estimator 88. The output of the $Q_{component}$ DC estimator 104 is fed into a $Q_{component}$ DC averager 106, which calculates a time-average of its DC input using, for example, techniques described above with respect to the $Q_{component}$ DC averager 90.

[0015] The output of the $Q_{component}$ DC averager 106 is fed into the DC component subtracter 102, which subtracts the time-averaged DC component from the demodulated quadrature-phase $Q_{component}$ signal on line 98. The output of the DC component subtracter 102 $Q'_{component}$, which represents the $Q_{component}$ value having any DC offset that may be contained therein substantially removed, then is fed into the symbol demodulator and decoder 96.

[0016] The systems, functions, and operations described in the block diagrams, graphs, or examples above may be implemented, individually or collectively, in hardware, software, firmware, or a combination thereof. For example, the functions may be implemented in application specific integrated circuits (ASICs), standard integrated circuits, as one or more computer programs running on a computer, computer system, one or more controllers (e.g., microcontrollers), one or more processors (e.g., microprocessors), or any combination thereof. In addition, the processes, methods, or techniques of the invention may be distributed as a program product in a variety of forms, such as may be incorporated in a digital storage medium, or the like.